REMARKS

Claim 20 is amended, no claims are canceled, and no claims are added; as a result, claims 1-23 are now pending in this application.

No new matter has been introduced through the amendments to claim 20. Support for the amendments to claim 20 may be found throughout the specification, including but not limited to the specification on page 3, lines 5-12 and in FIG. 1.

§103 Rejection of the Claims

Claims 1-20

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Arcoleo et al. (U.S. 5,864,506) in view of Marshall et al. (U.S. 6,876,224). Applicants do not admit that Marshall et al. is prior art and reserve the right, as provided for under 37 C.F.R. 1.131, to "swear behind" Marshall et al. at a later time. However, it is unnecessary to swear behind Marshall et al. at this time because claims 1-20 are not obvious in view of the proposed combination of Arcoleo et al. and Marshall et al. Applicants respectfully traverse the rejection of claims 1-20.

Claims 1-20 are not obvious in view of the proposed combination of Arcoleo et al. and Marshall et al. because the proposed combination of Arcoleo et al. and Marshall et al. fails to disclose or suggest all of the subject matter included in claims 1-20. By way of illustration, independent claim 1 includes:

> a first circuit coupled to an input port of the transmitter, the first circuit including a single input port and a single output port and **no more than two transistors including a first transistor and a second transistor, the first transistor having a source/drain directly connected to a source drain of the second transistor, the second transistor larger than the first transistor.** (Emphasis added).

Thus, the subject matter of independent claim 1 includes a first circuit having "no more than two transistors including a first transistor and a second transistor, the first transistor having a source/drain directly connected to a source drain of the second transistor, the second transistor larger than the first transistor." There is no disclosure or suggestion in either Arcoleo et al. or in Marshall et al. of at least this subject matter as included in independent claim 1.

In an attempt to supply this subject matter, the Office Action refers to Arcoleo et al. as stating,[1]

> As can be readily appreciated by those skilled in the art, **the particular magnitudes of the output buffer drive strengths** (i.e., the amount of current that can be sourced to or from the output node 404) produced by the output buffer circuits of FIGS. 5A and 5B are dependent upon the physical characteristics of the inverters 501 and 502. In particular, in **the output buffer circuit of FIG. 5B, the drive strengths are determined by the physical characteristics (e.g., length, width, capacitance, channel resistance) of the transistors 501a, 501b, 502a and 502b.** Thus, by appropriately selecting the physical characteristics of the transistors 501a, 501b, 502a and 502b, the possible drive strength magnitudes can be predictably established. (Emphasis added).

Here, Arcoleo et al. describes magnitudes of the output buffer drive strength as being determined by the physical characteristics of the transistors 501a, 501b, 502a, and 502b. However, there is no description of any of these transistors having a size that is *different* from any other one of these transistors. The text of Arcoleo et al. merely states that by determining the physical characteristics of the transistors, the possible drive strength magnitudes can be predictably established. According to this description *a same* length, width, capacitance, or channel resistance for transistors 501a, 501b, 502a, and 502b could be selected to provide a possible drive strength magnitude. However, these statements in Arcoleo et al. fail to disclose or suggest the first circuit including, "no more than two transistors including a first transistor and a second transistor, the first transistor having a source/drain directly connected to a source drain of the second transistor, **the second transistor larger than the first transistor**," as required by independent claim 1. (Emphasis added).

In further support of these statements, attention is directed to the specification of the application, which states,[2]

> Referring again to Fig. 1 and Fig. 2, in some embodiments, the sizing of the first circuit 106 includes sizing the *p*-type metal-oxide semiconductor field-effect transistor 202 and the *n*-type metal-oxide semiconductor field-effect transistor 204 included in the inverter 200. In some embodiments, the *n*-type metal-oxide

[1] *See* the Office Action for example on page 3, line 3 referencing Arcoleo et al. at column 8, lines 22-26.
[2] *See* Applicants' specification at page 4, lines 15-22.

> semiconductor field-effect transistor 204 is sized to be larger than the *p*-type metal-oxide semiconductor field-effect transistor 202. **Sizing the *n*-type metal-oxide semiconductor field-effect transistor 204 larger than the *p*-type metal-oxide semiconductor 202 compensates for a slow response in the second circuit 108.** (Emphasis added).

Thus, the sizing of the second transistor larger than the first transistor in the first circuit of independent claim 1 allows compensation for a slow response that might occur in the second circuit included in independent claim 1. The text from Arcoleo et al. referred to in the Office Action as describing this subject matter makes no mention of compensation for slow responses, but merely discusses "drive strengths (i.e., the amount of current that can be sourced to or from the output node 404)." There is no discussion in Arcoleo et al. of compensation for slow response times with respect to the selection of characteristics for transistors in Arcoleo et al. Therefore, Arcoleo et al. fails to disclose or suggest the first circuit wherein, "the first transistor having a source/drain directly connected to a source drain of the second transistor, **the second transistor larger than the first transistor,**" as required by independent claim 1. (Emphasis added).

In further illustrations of subject matter included in claims 1-20 and not disclosed or suggest by Arcoleo et al., claim 4, which depends from independent claim 1 includes,

> wherein the n-type metal-oxide semiconductor field-effect transistor is larger than the p-type metal-oxide semiconductor field-effect transistor.

In addition, claim 5, which also depends from independent claim 1 includes,

> wherein the n-type metal-oxide semiconductor field-effect transistor is between about two and about three times larger than the p-type metal-oxide semiconductor field-effect transistor.

In rejecting claim 4, the Office Action relies on the above quoted portion of Arcoleo et al.[3] However as noted above, this portion of Arcoleo et al. fails to disclose or suggest "the first transistor having a source/drain directly connected to a source drain of the second transistor, the second transistor larger than the first transistor," as included in independent claim 1. Further,

[3] *See* the Office Action on page 4, referring to Arcoleo et al. at column 8, lines 20-26.

there is no disclosure or suggestion of any of the transistors 501a, 501b, 502a, and 502b having any difference in size for these transistors based on the *different types* of transistor. Therefore, there is no disclosure or suggestion in Arcoleo et al. of, "wherein the n-type metal-oxide semiconductor field-effect transistor is larger than the p-type metal-oxide semiconductor field-effect transistor," as included in claim 4.

For analogous reasons, Arcoleo et al. fails to disclose or suggest, "wherein the n-type metal-oxide semiconductor field-effect transistor is between about two and about three times larger than the p-type metal-oxide semiconductor field-effect transistor," as included in claim 5. In rejecting claim 5, the Office Action relies on MPEP 2144.04 IV. A. and states,[4]

> In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, **where the only difference** between the prior art and the claims was a recitation of relative dimensions of the claimed device **and a device having the claimed relative dimensions would not perform differently** than the prior art device, the claimed device was not patentably distinct from the prior art device.
>
> Therefore, simply changing the size of the transistors does not change the operation of the circuit to give it patentable weight over the prior art. (Emphasis added).

However, Applicants respectfully submit that the recitation of "the first transistor having a source/drain directly connected to a source drain of the second transistor, the second transistor larger than the first transistor," does change the operation of the circuit, wherein as noted above in Applicants' specification,[5] "Sizing the *n*-type metal-oxide semiconductor field-effect transistor 204 larger than the *p*-type metal-oxide semiconductor 202 compensates for a slow response in the second circuit 108." Thus, the case law referred to in MPEP 2144 IV. A. does not properly apply to the subject matter included in independent claim 1 as compared to Arcoleo et al. Further, there is no disclosure or suggestion of the subject matter included in claim 5, either in Arcoleo et al. or any other evidence made of record provided in the Office Action.

In a still further illustration of subject matter included in the claims and not disclosed or suggested by Arcoleo et al., claim 11 includes,

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[4] *See* the Office Action on page 4, third paragraph.
[5] *See* Applicants specification at page 4, lines 20-22.

> The transmitter of claim 1, wherein the transmitter transmits at a signal level and the first circuit and the second circuit are coupled to a supply potential having a value of about twice the signal level.

In rejecting claim 11, the Office Action states,[6]

> Regarding claim 11, the combination discloses where the transmitter transmits at a signal level and the first circuit and the second circuit are coupled to a supply voltage potential (Vcc) having a value about twice the signal level (the transmit voltage will be lower than the supply voltage based on the physical size of transistors 604-607a. The combination between the value of the supply voltage and the physical size of the transistors can make the voltage supply about twice that of the transmission voltage).

While Applicants do not agree with any of these statements, the statements in and of themselves fail to point out in Arcoleo et al. (and in Marshall et al.) where the subject matter included in claim 11 is found. The Office Action also fails to point out in Arcoleo et al. (or in Marshall et al.) or by any other evidence of record, where the statements made in the Office Action in rejecting claim 11 may be found. Further, the Office Action fails to point to any evidence as to how these statements would be generally known by those of ordinary skill in the art. Without such a showing, the Office Action fails to meet its burden for establishing a *prima facie* case of obviousness with respect to claim 11.

Applicants' representatives fail to find in, and the Office Action fails to point out in Marshall et al., where there is a disclosure or a suggestion of the subject matter described above as included in independent claim 1 and in claims 4, 5, and 11 and missing from Arcoleo et al. Therefore, the Office Action failed to show how the proposed combination of Arcoleo et al. and Marshall et al. discloses or suggests all of the subject matter included in independent claim 1 and in claims 4, 5, and 11. Thus, the Office Action failed to meet its burden for establishing a *prima facie* case of obviousness with respect to independent claim 1 and claims 4, 5, and 11.

In further examples of subject matter included in claims 1-20 and not disclosed or suggested by the proposed combination of Arcoleo et al. and Marshall et al.:

Independent claim 12 includes,

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[6] *See* the Office Action at page 5, fourth paragraph.

> receiving a signal at a first circuit, the first circuit including an input port and an output port and no more than two transistors including a first transistor and a second transistor, the first transistor having a source/drain directly connected to a source drain of the second transistor, **the second transistor larger than the first transistor**. (Emphasis added).

Independent claim 16 includes,

> a first circuit coupled to an input port of the transmitter, the first circuit including an input port and an output port and no more than two transistors including a first transistor and a second transistor, the first transistor having a source/drain directly connected to a source drain of the second transistor, **the second transistor larger than the first transistor**. (Emphasis added).

For reasons analogous to those stated above with respect to independent claim 1, the proposed combination of Arcoleo et al. and Marshall et al. fails to disclose or suggest all of the subject matter included in independent claims 12 and 16, and so the Office Action fails to meet its burden for establishing a *prima facie* case of obviousness with respect to independent claims 12 and 16.

Claims 2-11, 13-15, and 17-19 depend from one of independent claims 1, 12, and 16, and so include all of the subject matter included in the independent claim from which they depend, and more. For at least the reasons stated above with respect to independent claims 1, 12, and 16, and for at least the reasons stated above with respect to claims 4, 5, and 11, the proposed combination of Arcoleo et al. and Marshall et al. fails to disclose or suggest all of the subject matter included in claims 2-11, 13-15, and 17-19. Therefore, the Office Action fails to meet its burden for establishing a *prima facie* case of obviousness with respect to claims 2-11, 13-15, and 17-19.

In another example of subject matter included in claims 1-20 and not disclosed or suggested by the proposed combination of Arcoleo et al. and Marshall et al., independent claim 20 as amended includes,

> A system comprising:
> a first processor including a transmitter comprising:

> **a first circuit including a single and no more than one input port coupled to an input port of the transmitter and a single and no more than one output port; and**
>
> **a second circuit including a single and no more than one second circuit input port directly coupled only to the single and no more than one output port of the first circuit,** the second circuit including a second circuit output port coupled to an output port of the transmitter, wherein the first circuit is sized with respect to the second circuit such that for a pulse signal applied to the input port, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at the output port; and
>
> a second processor including a receiver coupled to the transmitter through a transmission line.

Thus, in independent claim 20 the first circuit includes no more than one input port coupled to an input port of the transmitter, and the second circuit includes a single and not more than one second circuit input port directly coupled only to the single and no more than one output port of the first circuit.

In contrast to independent claim 20, Arcoleo et al. states,[7]

> The output buffer circuit of FIG. 6 includes three inverters 603, 604 and 605, each of which are implemented by a P-channel pull-up transistor (transistors 603a, 604a and 605a, respectively) connected in series with an N-channel pull-down transistor (transistors 603b, 604b and 605b, respectively) between a supply voltage and a ground voltage. **The gate of each of the transistors 603a, 603b, 604a, 604b, 605a and 605b is electrically connected to the input node 601, so that an input signal received at the input node 601 controls the current flow through the transistors 603a, 603b, 604a, 604b, 605a and 605b to produce a predictable output signal at the output node 602, as described above.** (Emphasis added).

Thus, Arcoleo et al. describes coupling all of the gates of the transistors 603a, 603b, 604a, 604b, 605a and 605b to the input node 601, and so fails to disclose or suggest the first circuit and the second circuit including, "a second circuit including a single and no more than one second circuit input port directly coupled only to the single and no more than one output port of the first circuit," as required by independent claim 20.

[7] *See* Arcoleo et al. at column 8, lines 54-65.

In further contrast to the subject mater of independent claim 20, Marshall et al. shows in Figure 2 each of transistors 206, 208, 210, 226, 228, and 230 as having gates individually connected to edge timing logic 220.[8] Thus, Marshall et al. also fails to disclose or suggest the first circuit and the second circuit including, "a second circuit including a single and no more than one second circuit input port directly coupled only to the single and no more than one output port of the first circuit," as required by independent claim 20.

For at least the reasons stated above, the proposed combination of Arcoleo et al. and Marshall et al. fails to disclose or suggest all of the subject matter included in independent claim 20, and so independent claim 20 is not obvious in view of the proposed combination of Arcoleo et al. and Marshall et al.

Applicants respectfully request reconsideration and withdrawal of the rejection, and allowance of claims 1-20.

Claims 21-23.

Claims 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Arcoleo et al. (U.S. 5,864,506) in view of Marshall et al. (U.S. 6,876,224) in further view of Song (U.S. 6,614,258). Applicants respectfully traverse the rejection of claims 21-23.

Claims 21-23 depend from independent claim 20, and so include all of the subject matter included in independent claim 20, and more. Applicants believe they have established for at least the reasons stated above that independent claim 20 is not obvious in view of the proposed combination of Arcoleo et al. and Marshall et al. because neither Arcoleo et al. nor Marshall et al., either alone or in any combination, disclose or suggest all of the subject matter included in independent claim 20. The addition of Song fails to remedy the deficiencies of Arcoleo et al. and Marshall et al., and so the proposed combination of Arcoleo et al., Marshall et al., and Song also fails to disclose or suggest all of the subject matter included in claims 21-23.

For at least the reasons stated above, claims 21-23 are not obvious in view of the proposed combination of Arcoleo et al., Marshall et al., and Song.

Applicants respectfully request reconsideration and withdrawal of the rejection, and allowance of claims 21-23.

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[8] *See* Marshall et al. at column 3, line 31-61 and at Figure 2.

Reservation of Rights

In the interest of clarity and brevity, Applicants may not have addressed every assertion made in the Office Action. Applicants' silence regarding any such assertion does not constitute any admission or acquiescence. Applicants reserve all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicants do not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicants timely object to such reliance on Official Notice, and reserve all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicants reserve all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney ((612)-371-2132) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 21st day of June 2007.

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Signature